REMARKS

I. Status of Claim

Claims 1, 3-11 and 14-16 are pending.

Claims 1, 3-11 and 14-16 stand rejected.

Claims 4, 5, 9 and 16 are objected to.

Claims 2, 12-13 were cancelled in a prior response.

Claims 3 and 9 have been cancelled herein.

Claims 1, 4, 5, 10, 15 and 16 are currently amended.

II. Objection to Amendment Format

The examiner has objected to certain errors in the format of the amendments made to the claims in the prior Office Action. Applicant, through his attorney, wishes to thank the examiner for his observations regarding the typographical errors. Applicant believes that the errors were not of a nature that would cause confusion in the intent of the amendments made. Applicant further believes that the amendments to the claims submitted in the prior response have been entered and has amended the claims herein to correct any other errors than may have been found.

III. Objection to the Claims

The examiner has object to claims 4, 5, 9 and 16 for containing informalities. Applicant, through his attorney, again wishes to thank the examiner for his observations and has made necessary amendments to the claims to correct the noted informalities.

Having made amended the claims to correct the informalities, applicant submits that the reasons for the examiner's objection to the claims have been overcome and can no longer be sustained. Applicant respectfully request that the objection be withdrawn.

IV. Rejection pursuant to 35 USC §112

The examiner has rejected claims 4 and 5 pursuant to 35 USC §112, first paragraph, "because the specification, while enabling for a dual processor system ... does not reasonably provide enablement for 'a first processor and at least one second processor,' i.e., there is no enablement for having more than one coprocessor." The examiner further rejected claim 8,

pursuant to 35 USC §112, first paragraph, "because the specification, while enabling for a dual processor system ... does not reasonably provide enablement for 'a system having many selectable devices such as other coprocessors.'"

Applicant respectfully disagrees with the examiner's rejection as the specification provides clearly contemplates multiple devices such as co-processors by stating "[s]ystem address bus 142 is used to select a particular device in computer system 100, e.g., to select co-process 120 in a system having many selectable devices such as other co-processors (not shown) or to select control register 121 of co-processor 120 where control register 121 is one of several other addressable units (not shown) of co-processor 120."[p.3, lines 14-20]. Accordingly, one enable one skilled in the art would understand that the control register can be used to address other addressable units in the system and even particular addressable sub-units within a selected unit by using an addressing/sub-addressing scheme I the system address bus. Although the written description describes the present invention with regard to a dual processor system, the inventive concept is in the dynamic operation of the selected unit, e.g., co-processor, in responding to the burst operation. Hence, the manner and method of selection of multiple units need not be described in the written description.

Having shown that a multi-processing system, as described in the specification, was contemplated by the applicant, applicant submits that the examiner's reason for rejecting the claims has been overcome.

Applicant respectfully requests the rejection be withdrawn and the claims allowed.

V. <u>Rejection pursuant to 35 USC §102</u>

The examiner has rejected claims 1, 3-11 and 14-16 as being anticipated by Campanini U.S. Patent No. 4,700,292 (Campanini or '292). It is the examiner's position that with regard to independent claim 1 "Campanini has taught a dual processor system," including all the elements recited in the claim. The examiner has specifically referred to Fig. 1, Fig. 5(component El_b), col. 9, lines 27-34, Fig. 4, col. 2, lines 33-38 and col. 8, line 61 to col. 9, line 10. The examiner has further provided an example how the word count recited by Campanini may be used as a burst mode indicator.(see page 6, Office Action dated 12/24/2003 [OA hereinafter]). More specifically, the examiner states that the word counter of Campanini may have a dual use when

used as a burst mode indicator. For example, using an X-bit word counter, the leading X-1 bits may be used as burst mode indicator when any bit other than the "1" bit is set.

With regard to claims 3-16, it is the examiner's position that Campanini has taught a dual processor system as described in claim 1 and the subject matter recited in the aforementioned claims.

The applicant, through his attorney, wishes to thank the examiner for the further clarification of the rejection of the claims in his Response to Arguments beginning on page 12 of the Final Office Action. With regard to claim 1, the examiner rationalizes that because "applicant has made use of the term 'comprising' within claim 1," and "'the term comprises is inclusive and fails to exclude un-recited steps" and "[t]he applicant has never explicitly excluded this counter component and the term 'comprising' with the claim allows extra steps (or components) to exist within the prior art." (see page 13, item 27). The examiner further provides an example of the above rational in the following example; "if the present invention claims feature 'A', and Campanini [the prior art reference cited] has taught features 'A,' 'B,' and 'C,' then Camanini still reads on the claims." (see page 14, item 31).

With regard to claim 3, it is the examiner's position that "Campanini taught a dual processor systems as described in claim 1. Campanini has further taught that the second process remains in the burst mode only so long as the first processor asserts the data register system address on the system address bus. ... [t]he WR signal is asserted just before each incoming word arrives via bus BC and is stored in the data register ... As long as the data register system address signal WR is applied, then data still needs to be transferred. Once there is no data left to transfer, the WR signal will not be applied and burst mode will be finished. If the WR signal is no longer asserted, then clearly no more incoming data is arriving." [emphasis added].

With regard to claims 4-11 and 14-16, the examiner rejected these claims based on the rejection of claim 1, as "Campanini has taught a dual processor system as described in claim 1. Campanini has further taught ..."

Applicant respectfully disagrees with and explicitly traverses the examiner's reasons for rejecting the claims as being anticipated by Campanini. However, in the interest of advancing the prosecution of this matter, applicant has amended the claims to more clearly recite the invention claimed. More specifically, applicant has amended each of the independent claims to

clearly recite that the selected secondary unit remains in burst mode "so long as said first processor asserts the data register system address on the system address bus."

It is well recognized that to constitute a rejection pursuant to 35 USC 102, i.e., anticipation, all material elements recited in a claim must be found in one unit of prior art. For reasons shown below, Campanini does not anticipate the present invention because Campanini does not include each and every element recited in the claims.

As support for the examiner' argument that the present invention as recited in claim 1 is anticipated by Campanini, the examiner cites Campanini, the "header data is sent prior to the actual data words that are to be transferred. See abstract. This header includes the number of words to be transferred and the starting destination address." (See page 6 first full paragraph, OA). As the examiner further notes, Campanini writes a starting address and a word count and then counts the words downward while incrementing memory.

However, *the present invention has no component for a word counter or for the decrementation of a numerical value stored in a word counter. Rather only a starting address for the subsequent data storage is necessary as memory accesses and corresponding write signals move the data into contiguous memory locations.*

The examiner further points out that Campanini utilizes the "...arrival of each writing command WR at signal receiver RIS (FIG. 4), which *immediately precedes* each incoming data word, causes the incrementation of the contents of register MEA and the decrementation of the numerical value stored in word counter ..", as indicative of the '292 WR signal acting as a system address for the data register. However, *in the present invention, there is no signal proceeding each incoming data word. Rather the mere presence of data on the address bus is sufficient to indicate that data is present.*

The examiner notes that the word counter may be used as a burst mode indicator. It is the examiner's position that in using an X-bit word counter, the setting of any of the leading X-1 bits may be used to indicate a burst mode. (see page 6, last paragraph, page 10-11, paragraph 19, and page 16, paragraph 36, OA). However, applicant respectfully submits that the suggested use of the word counter as a burst indicator is one manner of constructing or implementing the invention. However, this construction does not anticipate the invention as recited in amended claim 1.

Table 1 illustrates the logic suggested by the examiner as an example of the word counter used as a burst mode indicator for a word count value of four (4).

Word Count Value	Binary Representation	Mode
4	0000100	Burst
3	0000011	Burst
2	0000010	Burst
1	0000001	Non-Burst, No bits other that single data transfer bit set.

Table 1: Example of Dual-Use Word Count Values

Thus, as illustrated, using the word count concurrently as a word counter and a burst indicator would fail to maintain the co-processor in a burst mode when the word counter decreases to the value of one (1). Hence, contrary to the examiner's position that "[o]nce there is no data left to transfer, the WR signal will not be applied and burst mode will be finished," the dual use of the word counter would fail to maintain the device of Campanini in the burst mode while one more piece of data is left to be transferred.

Hence, applicant respectfully submits that the dual use of the word counter as suggested by the examiner does not anticipate the step that the co-processor remains in the burst mode "so long as said first processor asserts the data register system address on the system address bus," as is recited in the claims. Furthermore, as one skilled in the art would recognize, while dual-use of registers, counters, or signals may be attractive, such use tends to introduce further complexities in order to maintain such dual-use as the operation or requirements of the register, counter or signal change to meet other needs. Hence, one skilled in the art would tend to shy away from such dual uses.

Finally, the examiner has further stated that because the claims use the open-ended term "comprising" that the use of a word counter is not precluded from being included in the present invention. Under this logic, if a patent could be obtained for a liquid containing the elements coffee, sugar, and milk would anticipate a patent application for a liquid containing only the element coffee, even if the elements of sugar and milk are not positively recited. The applicant submits that in this case neither the claims nor the specification refer to the use of a word

counter. More specifically, the written description, on page 4, lines 1-13, describes how the present invention fails to require the extra hardware lines and complexity necessary to provide both separate address and data busses, which are common in conventional processor-to-processor transfers. Hence, there is no teaching that would encompass a word counter as being included in the novel concept of the present invention.

Regarding claim 3, as noted above in Table 1, the dual use of a word counter as a word counter and a burst mode indicator does not retain the device of Campanini in the burst mode until no more data is transferred. Rather, the Campanini device would exit the burst mode with at least one more piece of data yet to be transferred. Accordingly, the dual use word counter, suggested by the examiner and not discussed or described by Campanini fails to anticipate the subject matter that was recited in claim 3, now cancelled, and included in claim 1.

With regard to claims 4-11 and 14-16, these claims have been rejected either as being anticipated by Campanini for the same reasons as recited in claim 1 or that they depend from an independent claim that has been rejected as being anticipated by Campanini. Accordingly, the remarks made with regard to claims 1 and 3 are applicable to overcome the rejection recited with regard to claims 4-11 and 14-16 and are thus repeated as if restated in their entirety. Hence, for the same remarks made with regard to claims 1 and 3, application submits that claims 4-11 and 14-16 are also allowable over the Campanini reference cited.

For the amendments made to the claims and remarks made herein applicant submits that the reason for the examiner's rejection of the claims has been overcome and can no longer be sustained. Applicant respectfully requests that the amendments made be entered, reconsideration of this application in view of the amendments and allowance of the claims.

VI. Support for the amendments

Support for the amendments to the independent claims made herein is provided in the dependent claims 3 and 9 and Table 1 on page 4 of the written description. No new matter has been added.

VII. Telephonic Interview

Applicant, through his attorney, wishes to thank the examiner for taking the time to conduct a telephonic interview wherein the examiner, in view of a proposed set of claims and remarks provided by applicant, clarified his position that the use of a word counter as a burst mode indicator occurred upon the initial transfer of the word counter and not on subsequent decrementing of the transferred word counter.

No agreement was reached with regard to the proposed amendments to the claims. However, applicant has amended the claims, herein, to make clear that the operations of the co-processor are performed independent of a number of words to be exchanged between the between processors.

VIII. Conclusion

Having addressed the examiner's rejections under 35 USC § 102 (b), applicant submits that for the amendments and remarks made herein the reasons for the examiner's rejections have been overcome and can no longer be sustained. Applicant respectfully requests reconsideration and withdrawal of the rejections and that a Notice of Allowance be issued.

Please inform the applicant, through his attorney, if the examiner differs in that view. Should any unresolved issues remain, the examiner is invited to call Applicant's attorney at the telephone number below.

IX. Fees

This firms check for the payment of fees for filing this Request for Continued Examination is included. No other fees are believed necessary. However, the Commissioner for Patents is hereby authorized to charge any additional fees, including fees for extensions of time or credit any excess payment that may be associated with this communication to Duane Morris LLP deposit account 50-2061.

Respectfully submitted,

DUANE MORRIS, LLP

By _____

Carl A. Giordano.
Reg.No. 41780

Duane Morris LLP
380 Lexington Avenue
New York, NY 10168
212.692.1078
212.692.1020 (fax)